ABSTRACT:

A multi-issue processor comprises a plurality of issue slots ($UC_0$, $UC_1$, $UC_2$ and $UC_3$), each one of the plurality of issue slots having a plurality of functional units ($FU_0$, $FU_1$ and $FU_2$) and a plurality of holdable registers (1 – 33 and 101 – 117). The plurality of issue slots comprises a first set of issue slots ($UC_1$, $UC_2$ and $UC_3$) and a second set of issue slots ($UC_0$), and the register file ($RF_0$ and $RF_1$) is accessible by the plurality of issue slots ($UC_0$, $UC_1$, $UC_2$ and $UC_3$). A location of at least a part of the plurality of holdable registers (1 - 33) in the first set of issue slots ($UC_1$, $UC_2$ and $UC_3$) is different from a location of at least a corresponding part of the plurality of holdable registers (101 - 117) in the second set of issue slots ($UC_0$). The holdable registers can prevent that the inputs of unused functional units change, which would result in unnecessary power dissipation. However, this increases the amount of state that has to be saved during interrupt handling. By varying the position of the holdable registers for different issue slots, less state saving may be required during interrupt handling, while maintaining a significant reduction in power consumption and improved performance.

Fig. 3